WHAT IS CLAIMED IS:

1. A deep submicron electrostatic discharge (ESD) protection structure comprising:

first and second electrodes separated by a dielectric material;

a source positioned proximate to the first electrode; and

a drain positioned proximate to the first electrode and covered by a silicide layer, wherein the silicide layer enhances ESD protection provided by the structure.

2. The structure of claim 1 wherein the dielectric material comprises a thin oxide layer of less than 25 Å.

3. The structure of claim 2 wherein the first electrode forms a channel with a length of approximately 900 μm and a width of approximately 0.25 μm.

4. The structure of claim 1 wherein the silicide layer is a metal silicide.

5. The structure of claim 4 wherein the metal silicide is formed using at least one of titanium, tungsten, cobalt, and nickel.

6. The structure of claim 1 wherein the structure is an n-channel metal oxide semiconductor field effect transistor.

7. The structure of claim 1 wherein the structure is a p-channel metal oxide semiconductor field effect transistor.

8. The structure of claim 1 wherein the drain is floating, and wherein the floating drain modifies the ESD protection provided by the structure.

9. The structure of claim 8 further comprising a parasitic element formed by current interactions between the source, the floating drain, and a doped area.

10. The structure of claim 9 wherein the parasitic element functions as a bipolar junction transistor (BJT), and wherein the floating drain provides a constant potential region at the base of the BJT.

11. The structure of claim 1 wherein the structure is associated with a transition time from breakdown to snapback, and wherein the silicide layer shortens the transition time.

12. A deep submicron electrostatic discharge (ESD) protection structure for a deep submicron integrated circuit, the structure comprising:

a first finger having first and second electrodes separated by a thin oxide material, and a first source positioned proximate to the first electrode; and

a second finger having third and fourth electrodes separated by a thin oxide material, and a second source positioned proximate to the third electrode;

a drain positioned proximate to the first and third electrodes, and separated from the first source by the first electrode and from the second source by the third electrode; and

a silicide layer in direct contact with the drain.

13. The structure of claim 12 wherein the thin oxide material is less than 25 Å thick.

14. The structure of claim 13 wherein at least one of the first and third electrodes forms a channel with a length of approximately 900 μm and a width of approximately 0.25 μm.

15. The structure of claim 12 wherein the silicide layer is a metal silicide.

16. The structure of claim 15 wherein the metal silicide is formed using at least one of titanium, tungsten, cobalt, and nickel.

17. The structure of claim 12 wherein the silicide layer shortens a transition time of the structure from breakdown to snapback.

18. A method for fabricating a deep submicron electrostatic discharge structure, the method comprising:

forming a well region;

forming a thin gate oxide layer above the well region;

forming a polysilicon gate structure above the gate oxide layer;

forming a source region proximate to the gate oxide layer;

forming a drain region proximate to the gate oxide layer and opposite the source region; and

forming a silicide layer over the drain region.

19. The method of claim 18 wherein forming the thin gate oxide layer includes depositing an oxide of less than 25 Å thick.

20. The method of claim 18 wherein forming the silicide layer includes laying down a metal silicide using at least one of titanium, tungsten, cobalt, and nickel.

21. The method of claim 18 further comprising forming a silicide layer over the source region.

22. The method of claim 18 further comprising

covering the polysilicon gate structure, the source region, and the drain region with a dielectric layer; and

forming, through the dielectric layer, a first interconnection to the source region and a second interconnection to the polysilicon gate structure, while leaving the dielectric layer above the drain region intact, wherein the drain region is not connected to an interconnection and is floating.